REMARKS/ARGUMENTS

Claims 1, 2 and 4-10 remain in the application. Of these, claims 1, 2, 4 and 6-10 stand rejected. Claim 5 stands objected to as being dependent on a rejected claim, but is otherwise allowable. Claim 3 has been canceled.

1. Objection to the Drawings

The Drawings stand objected to under 37 CFR 1.83(a), because the Examiner asserts that, "in claims 3 and 4, the matched delays implemented as differential pairs or matched traces must be shown or the feature(s) canceled from the claim(s)." See, 5/16/2007 Office Action, p. 2, sec. 1.

Although applicant believes that one of ordinary skill in the art would readily know and understand various ways of implementing matched delays using differential pairs, applicant believes the selection of any particular one of these implementations, for illustration in the drawings, would be a somewhat arbitrary undertaking. That is, although applicant believes claim 3 is fully supported and enabled by the written description, applicant believes the illustration of a particular embodiment of the subject matter of claim 3 might raise a question regarding new matter. As a result, applicant has canceled claim 3 at this time (without prejudice).

With respect to claim 4, applicant believes the implementation of matched delays using matched traces is so well understood that the illustration of such a feature is unnecessary. Applicant also notes that traces do not necessarily need to look identical to be "matched", meaning that the traces shown in FIG. 3 could in some cases be considered "matched". As a result, applicant asks that the Examiner reconsider and withdraw his objection to the drawings with respect to claim 3.

2. Rejection of Claims 1, 2 and 6-10 under 35 USC 103(a)

Claims 1, 2 and 6-10 stand rejected under 35 USC 103(a) as being unpatentable over Evans et al. (US Pat. 6,002,279; hereinafter "Evans") in view of Mooney et al. (US Pub. Pat. App. 2003/0002607; hereinafter "Mooney").

The Examiner asserts that, in FIG. 7A (elements 702, 704), and in col. 4, line 66 - col. 5, line 16, Evans teaches all of the elements of claim 1 but for a clock interpolator and a current steering mechanism. However, the Examiner asserts that a clock interpolator and current steering mechanism are taught by Mooney, and that it would have been obvious to one of ordinary skill in the art, at the time of the invention, to combine Evan's and Mooney's teachings. Applicant disagrees.

With respect to claim 1's current steering mechanism, the Examiner asserts that Mooney teaches a current steering mechanism in par. [0032] and FIG. 4 (elements 420 and 450). The Examiner further asserts that "the steering [of] current between the first and second nodes is interpreted as being done by current sources 420 and 450." See, 5/16/2007 Office Action, p. 4, sec. 3. Applicant disagrees.

Applicant's claim 1 recites "a mechanism to steer current between first and second nodes, the first node being coupled to bias an input differential pair of the clock interpolator and a delayed differential pair of the data interpolator". In comparison, Mooney teaches that "the current sourced by current sources 420 and 450 is switched between the various differential transistor pairs" 402, 412, 432, 442. See, Mooney, par. [0032]. However, none of the differential pairs 402, 412, 432, 442 is a "delayed differential pair of a data interpolator", as recited in claim 1. In fact, it is noted that Mooney's FIG. 4 fails to teach a data interpolator of any kind, and Mooney's disclosure fails to teach how the current switching methodology implemented for the clock phase interpolator 400 would (or could) be integrated with both the clock phase interpolator 400 and a data interpolator. No guidance is provided by Evans, because Evans teaches independent clock and data paths.

Also, it is noted that Mooney's clock phase interpolator 400 is the output stage of a clock recovery circuit 100, as shown in Mooney's FIG. 1. As a result, it is unclear how the clock input 112 to the clock recovery circuit 100, and the clock 122/472

output from the clock phase interpolator 120/400, would be used to respectively operate first and second data sampling elements as recited in applicant's claim 1.

Applicant's claim 1 is believed to be allowable for at least the above reasons.

Claims 2, 4 and 6 are believed to be allowable, at least, because they depend from claim 1.

With respect to claim 7, the Examiner rejects this claim on the same basis that claim 1 is rejected. Similarly, applicant believes claim 7 to be allowable for reasons similar to why claim 1 is believed to be allowable.

Claims 8-10 are believed to be allowable, at least, because they depend from claim 7.

3. Rejection of Claim 3 under 35 USC 103(a)

Claim 3 stands rejected under 35 USC 103(a) as being unpatentable over Evans et al. (US Pat. 6,002,279; hereinafter "Evans") in view of Mooney et al. (US Pub. Pat. App. 2003/0002607; hereinafter "Mooney") and Lai et al. (US Pat. 5,012,494; hereinafter "Lai").

Given the cancellation of claim 3, this rejection is moot.

4. Rejection of Claim 4 under 35 USC 103(a)

Claim 4 stands rejected under 35 USC 103(a) as being unpatentable over Evans et al. (US Pat. 6,002,279; hereinafter "Evans") in view of Mooney et al. (US Pub. Pat. App. 2003/0002607; hereinafter "Mooney") and Simon et al. (US Pub. Pat. App. 2001/0053187; hereinafter "Simon").

Claim 4 is believed to be allowable, at least, because it depends from claim 1, because claim 1 is believed to be allowable for the reasons set forth in Section 2 of these Remarks/Arguments, and because Simon fails to teach that which is missing from Evans and Mooney.

5. Allowability of Claim 5

Applicant thanks the Examiner for indicating the allowability of claim 5 if rewritten in independent form. However, applicant has chosen to leave claim 5 in dependent form pending the Examiner's consideration of the remarks and arguments included herein.

6. Conclusion

In light of the amendments and remarks/arguments provided herein, applicant respectfully requests the issuance of a Notice of Allowance.

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